REMARKS

Amendments have been presented to claims 1, 7, 10, 17, and 21. Support for these changes is found throughout the specification.

35 U.S.C. 102(b) rejection

In the Office Action claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen.

The Applicants traverse these rejections of these claims.

Claim 1, as amended and with emphasis added as underlining, recites:

> A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:
> a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, each of said outbound bus transactions including a bus arbitration priority; and
> a first state machine coupled to the first and second outbound queues to service the first and second outbound queues by according the first queue a first outbound priority and the second queue a second outbound priority and serially requesting for access to the on chip bus for the staged outbound bus transactions based at least in part on accorded outbound priorities, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

Chen discloses, and the Examiner relies on, arbitration networks that use a first-in-first-out, multiple-requestor toggling (FIFO/MRT) system to insure that the oldest reference is processed first, and, in the case of multiple old references of the same age, a fairness algorithm ensures equal access to the ports connected to that arbitration network.

This is different from the language of claim 1 that recites that the first state machine will serially request for access to the bus based at least in part on outbound priorities, while access to the bus is granted based at least in part on bus arbitration priorities. It is clear from this language that there exists two different types of priorities,

e.g., a bus arbitration priority and an outbound priority. The outbound priorities may be used for determining the order in which the transactions will be processed by the state machine. While the bus arbitration priorities may be used for arbitrating bus access. So, for example, the state machine may determine that the first queue has a higher outbound priority and may therefore process transactions stored in that queue first. The state machine may pick a first transaction from the first queue, and make a request for the bus using the first transaction's bus arbitration priority. In one embodiment, a bus arbiter may grant bus access to a selected transaction, which could be the first transaction or a transaction from another subsystem, based at least in part on their bus arbitration priorities.

Chen, on the other hand, does not teach using these two different types of priorities. Once the arbitration network determines which request it intends to process first (based on FIFO/MRT) it simply sends that request over the path **50** which it has control over. Therefore, there is no request for bus access nor granting of bus access based on bus arbitration priority.

Furthermore, in the Examiner's response to Applicant's earlier argument, the discussion from Chen referring to replication of arbitration networks and queues for each of the memory ports is relied on to disclose the "particular feature of the second outbound data queue." If the Examiner uses these features in this manner, it is clear that the reference does not teach a state machine coupled to the first and second outbound queues, as recited in claim 1. Rather, this language simply teaches the replication of the circuitry disclosed in FIG. 44, e.g., additional arbitration networks and queues coupled to each other in the same manner arbitration network **320** is coupled to input port queue **324**. Without having the elements arranged as they are in the claims, this reference cannot be relied upon to anticipate this claim.

Because Chen does not include the above limitations, it does not anticipate this claim. Therefore, the Applicants respectfully request the Examiner to withdraw this rejection of this claim.

Claims 2-6 depend from, and include the same limitations as, claim 1. Therefore, these claims are patentably distinct from Chen for at least the above reasons and the Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claim 7, as amended, recites:

> A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:
>
> a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transactions including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and
>
> a state machine coupled to the first and second inbound queues to service the first and second inbound queues by according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority and serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem based at least in part on the accorded inbound priorities.

The Examiner relies on elements in Chen including input/output queues **352** and arbitration node **44** of FIG. 19a to anticipate claim 7. The Applicants respectfully traverses this rejection.

Similar to the above discussion, it is clear that Chen does not teach, suggest, or discuss a state machine serially bring staged transactions to the attention of a subsystem based at least in part on the inbound priorities it has accorded to the inbound queues. Furthermore, in Chen, access to the on-chip bus is not based at least in part on bus arbitration priorities, much less bus arbitration priorities that were chosen by the originating subsystems.

Because Chen does not include the above limitations, it does not anticipate this claim. Therefore, the Applicants respectfully request the Examiner to withdraw this rejection of this claim.

Claims 8-9 depend from, and include the same limitations as, claim 7 and are therefore patentably distinct from Chen for at least the same reasons as claim 7. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claims 10-16 include limitations similar those discussed above with reference to claim 1. For example, these claims include limitations directed to both outbound priorities and bus arbitration priorities. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons. Therefore, the Applicants respectfully request the Examiner withdraw these rejections of these claims.

Claims 17-20 include limitations similar to those discussed above with reference to claim 7. For example, these claims include limitations directed to inbound priorities and bus arbitration priorities. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons. Therefore, the Applicants respectfully request the Examiner withdraw these rejections of these claims.

Claim 21, for example, recites:

> In a subsystem of an integrated circuit, a method of operation comprising:
> determining intra-subsystem priorities for transactions with other subsystems of the integrated circuit to be serviced for requesting access to an on-chip bus of the integrated circuit, to which the subsystems are coupled;
> generating and staging the transactions in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit; and
> serially servicing the staged transactions in accordance with their intra-subsystem priorities, requesting access to the on-chip bus for each staged transaction being serviced using the included bus arbitration priority.

Similar to the above discussion, Chen does not teach, suggest, or discuss a subsystem serially servicing staged transactions according to their intra-subsystem

priorities, nor requesting access to the on-chip bus using the included bus arbitration priority.

Because Chen does not include the above limitations, it does not anticipate this claim. Therefore, the Applicants respectfully request the Examiner to withdraw this rejection of this claim.

Claims 22-24 depend from, and include the same limitations as, claim 21 and are therefore patentably distinct from Chen for at least the same reasons as claim 21. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claims 25-26 include limitations similar to limitations discussed above, including servicing staged transactions in accordance with the priority based manner (as requested by originating subsystems) and a bus arbitration priority, on which access to the on-chip bus was granted. Because Chen does not teach, suggest, or discuss these limitations, these claims are patentably distinct over Chen for at least these reasons.

Claim 27, for example, recites:

> An integrated circuit comprising:
> an on-chip bus; and
> a plurality of subsystems coupled to the on-chip bus and interact with each other through transactions conducted across said on-chip bus, with each of the subsystems having a data transfer interface that interfaces the subsystem to the on-chip bus, and at least one of the data transfer interfaces allows the particular subsystem to initiate transactions with other subsystems in a prioritized manner, including a first intra-subsystem prioritization on the order transactions contending for the service of the at least one of the data transfer interfaces are to be serviced, and a second inter-subsystem prioritization on the order transactions of the various subsystems contending for the on-chip bus are to be granted access to the on-chip bus.

Similar to the above discussion, Chen does not teach, suggest, or discuss a prioritization manner including a first intra-subsystem prioritization on the order transactions contending for the service of the at least one of the data transfer interfaces are to be serviced, and a second inter-subsystem prioritization on the order transactions

of the various subsystems contending for the on-chip bus are to be granted access to the on-chip bus.

Because Chen does not include the above limitations, it does not anticipate this claim. Therefore, the Applicants respectfully request the Examiner to withdraw this rejection of this claim.

Claims 28-31 depend from, and include the same limitations as, claim 27 and are therefore patentably distinct from Chen for at least the same reasons as claim 27. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claim 32 recites:

> In an integrated circuit having an on-chip bus and a plurality of subsystems coupled to each other via the on-chip bus, a method of operation comprising:
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> a first subsystem having a first data transfer interface interfacing the first subsystem to the on-chip bus, initiating first transactions with other subsystems through selective employment of facilities of the first data transfer interface to internally prioritizing the order the first transactions are to be serviced by the first data transfer interface, and including with said first transactions first bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including said first transactions; and
>
> a second subsystem having a second data transfer interface interfacing the second subsystem to the on-chip bus, initiating second transactions with other subsystems through selective employment of facilities of the second data transfer interface to internally prioritizing the order the second transactions are to be serviced by the second data transfer interface, and including with said second transactions second bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including the second transactions.

Similar to the above discussion, Chen does not teach, suggest, or discuss a subsystem to internally prioritize the order that transactions are to be serviced by the data transfer interface, and include bus arbitration priorities to facilitate prioritization of granting of access to on-chip bus.

Because Chen does not include the above limitations, it does not anticipate this claim. Therefore, the Applicants respectfully request the Examiner to withdraw this rejection of this claim.

Claims 33-35 depend from, and include the same limitations as, claim 32 and are therefore patentably distinct from Chen for at least the same reasons as claim 32. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

CONCLUSION

In view of the foregoing, the Applicant respectfully submits that claims 1-35 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2972.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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